ClearClock™ | Ultra-Low Jitter & Power Optimized 5.0 x 3.2 mm XO

AX5

ESD Sensitive

5.0 x 3.2 x 1.4 mm
RoHS/RoHS II Compliant
MSL = 1

Features

- Ultra-Low Jitter: 125 fs Typ RMS (200fs MAX, F>250MHz); spurs included
- Available with any frequency from 50MHz to 2100MHz
- Factory programmable; samples available within 1-2 week lead times
- Lowest in-class power consumption (60mA Typ LVDS)
- ±20ppm stability (-40 to +85ºC)
- 3.3V, 2.5V, 1.8V Vdd supply
- LVPECL, LVDS, HCSL, & CML differential output options
- Industry standard 5.0 x 3.2mm footprint

Applications

- Networking & communications
- 10G/40G/100G optical Ethernet
- RF systems, base stations (BTS)
- Datacenter
- PCI Express
- Test & measurement

Options and Part Identification [Note 1]

AX5 ▭ ▭ ▭ ▭ — ▭ ▭

(1): Output
- P: LVPECL
- D: LVDS (*)
- H: HCSL (**)
- M: CML (*)

(*) Frequency range limited to: 100~2100MHz
(**) Frequency range limited to: 50~700MHz

(2): V_{dd}
- A: 3.3V
- B: 2.5V
- C: 1.8V (*)

(*) Excluding LVPECL

(3): Stability over OTR
- D: ±15ppm over -20°C to +70°C
- F: ±20ppm over -40°C to +85°C

(4): OE Function
- 1: OE Pin 1; Active High
- 2: OE Pin 1; Active Low
- 3: OE Pin 2; Active High
- 4: OE Pin 2; Active Low

(5): Output Frequency in MHz

Please specify the frequency in units of MHz out to **4 digit** accuracy after the decimal.
Example:
"156.2500"=156.25000MHz

(6): Packaging
- Blank: Bulk (*)
- T: Tape & Reel 250 units

(*) MOQ: 25 units

Part Number Example:
AX5PAF1-644.53125

Note 1: Contact Abracon for non-standard part number configurations and/or requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal.

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ESD Sensitive

5.0 x 3.2 x 1.4 mm
RoHS/RoHS II Compliant
MSL = 1

Electrical Characteristics

Parameters			Min.	Typ.	Max.	Unit	Notes
Frequency Range	LVPECL		50		2100	MHz	Option "P"
	LVDS		100		2100		Option "D"
	HCSL		50		700		Option "H"
	CML		100		2100		Option "M"
Supply Voltage (V_{dd}) [Note 2]			2.97	3.3	3.63	V	Option "A"
			2.25	2.5	2.75		Option "B"
			1.71	1.8	1.89		Option "C"
Supply Current (I_{dd})	LVPECL			90	110	mA	Max @ 2100MHz; 3.3V
	LVDS			65	80		Max @ 2100MHz; 3.3V
	HCSL			77	90		Max @ 700MHz; 3.3V
	CML			69	85		Max @ 2100MHz; 3.3V
Operating Temperature Range			-20		+70	°C	Option "D"
			-40		+85		Option "F"
Storage Temperature			-55		+150	°C	
Frequency Accuracy (Initial Set-Tolerance) [Note 3] at time of shipment (Pre-Reflow) @ +25°C			-5.00	< ±3.00	+5.00	ppm	Relative to carrier
Frequency Stability over Operating Temperature Range			-15		+15	ppm	Over -20°C to +70°C
			-20		+20		Over -40°C to +85°C
Aging over 20 Year Product Life [Note 4,5]			-15		+15	ppm	
All-Inclusive Frequency Accuracy (Total Stability) over 20 Year Product Life [Note 4]			-40		+40	ppm	Over -20°C to +70°C
			-45		+45		Over -40°C to +85°C
Rise (Tr) / Fall (Tf) Time (20% to 80% $V_{peak\ to\ peak}$)					400	ps	
Duty Cycle			45		55	%	@ 50% V_{dd}
Powerup Time [Note 4]				< 5.0	10	ms	
Output High Voltage (V_{OH}) Output Low Voltage (V_{OL})	LVPECL	V_{OH}	V_{dd}-1.165		V_{dd}-0.8	V	50Ω to V_{dd}–2.0V or Thevenin equivalent
		V_{OL}	V_{dd}-2.0		V_{dd}-1.55		
	LVDS	V_{OH}		1.4	1.6		100Ω between OUT-P and OUT-N
		V_{OL}	0.9	1.1			
	HCSL	V_{OH}	0.66		1.15		50Ω to V_{dd}
		V_{OL}	0.0		0.15		
	CML	V_{OH}	V_{dd}-0.085		V_{dd}		50Ω to GND
		V_{OL}	V_{dd}-0.6		V_{dd}-0.32		
Output Enable & Disable Control			0.8*(V_{dd})			V	Output Enable; or No Connect
					0.2*(V_{dd})		Output Disable; High Impedance
Output Enable Time					2.5	ms	
Output Disable Time					10	µs	
Output Disable Current Consumption	LVPECL			85	100	mA	Max @ 2100MHz; 3.3V
	LVDS			60	70		Max @ 2100MHz; 3.3V
	HCSL			75	80		Max @ 700MHz; 3.3V
	CML			65	85		Max @ 2100MHz; 3.3V

Note 2: Supply Voltage (V_{dd}) = 1.8V option not available with LVPECL output
Note 3: Excludes carrier frequencies 122.88MHz, 491.52MHz, 368.4MHz, 614.4MHz, 737.28MHz, 860.16MHz, 983.04MHz, & 1105.92MHz. The Frequency Accuracy (Initial Set-Tolerance) at time of shipment (Pre-Reflow) for the above carrier frequencies = ±10ppm MAX.
Note 4: Relative to initial measured frequency @ +25°C
Note 5: Includes temperature stability, initial frequency accuracy, load pulling, power supply variation, and 20 year aging

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RoHS/RoHS II Compliant
MSL = 1

RMS Phase Jitter (12kHz -20MHz BW) | V_{dd} = 3.3V/2.5V/1.8V [Note 6,7,8]

Carrier F0 (MHz)	Min.	Typ.	Max.	Unit	Notes
251 to 2100		125	200	fsec	All Differential Outputs: LVPECL, LVDS, HCSL & CML
312.500000		125	145	fsec	LVPECL Output
322.265625		125	145	fsec	LVPECL Output
491.250000		115	135	fsec	LVPECL Output
622.080000		125	145	fsec	LVPECL Output
644.531250		115	135	fsec	LVPECL Output
1000.000000		115	135	fsec	LVPECL Output
1024.000000		125	145	fsec	LVPECL Output
1500.000000		110	130	fsec	LVPECL Output
2000.000000		130	150	fsec	LVPECL Output
2100.000000		130	150	fsec	LVPECL Output
126 to 250		150	300	fsec	All Differential Outputs: LVPECL, LVDS, HCSL & CML
150.000000		150	170	fsec	LVPECL Output
156.250000		130	160	fsec	LVPECL Output
200.000000		130	150	fsec	LVPECL Output
212.500000		125	145	fsec	LVPECL Output
250.000000		205	225	fsec	LVPECL Output
50 to 125		250	400	fsec	All Differential Outputs: LVPECL, LVDS, HCSL & CML
100.000000		150	170	fsec	LVPECL Output
122.880000		130	160	fsec	LVPECL Output
125.000000		130	150	fsec	LVPECL Output

Note 6: Guaranteed by characterization; RMS Phase Jitter specifications are inclusive of any spurs
Note 7: Phase jitter measured with Keysight E5052B Signal Source Analyzer not using a balun or buffer
Note 8: Refer to the next section for phase noise test setup and representative phase noise plots

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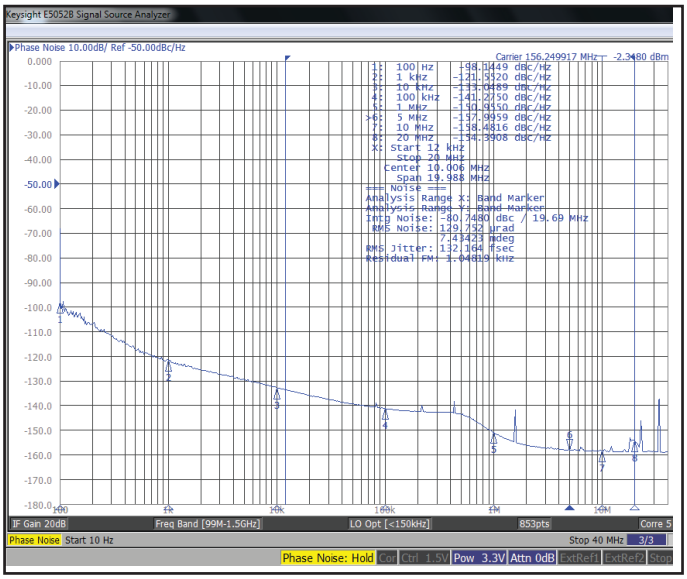
RoHS/RoHS II Compliant
MSL = 1

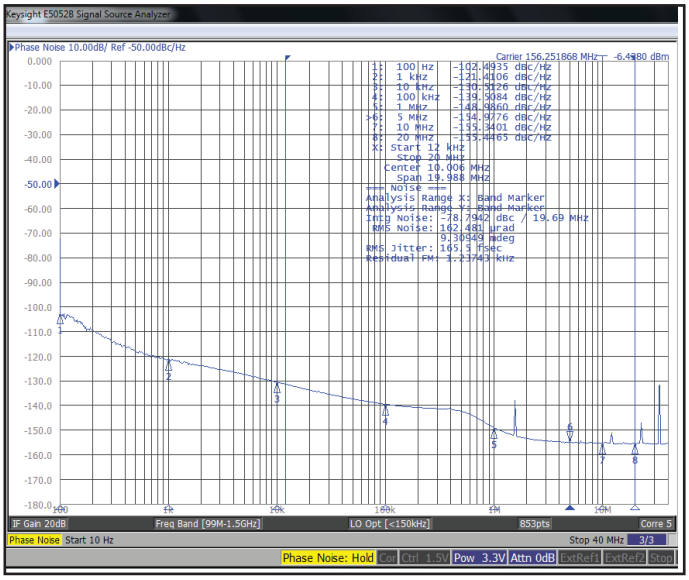
Phase Noise Test Setup [Note 9]

- Keysight E5052B Signal Source Analyzer
- Integration Bandwidth = 12kHz to 20MHz
- Spurious Activity (entire plot trace) = NOT Omitted (Normalized in dBc/Hz)
- Specifed Spur Omission Function = NOT Enabled
- IF Gain = 20dB
- Correlation = 5
- Average = 3

F=156.2500MHz
V_{dd}=3.3V
LVPECL
RMS Phase Jitter = 132 fsec



F=156.2500MHz
V_{dd}=3.3V
LVDS
RMS Phase Jitter = 165 fsec



Note 9: Contact Abracon for phase noise plots at any desired combination of V_{dd}, differential output format, and carrier frequency within the available range

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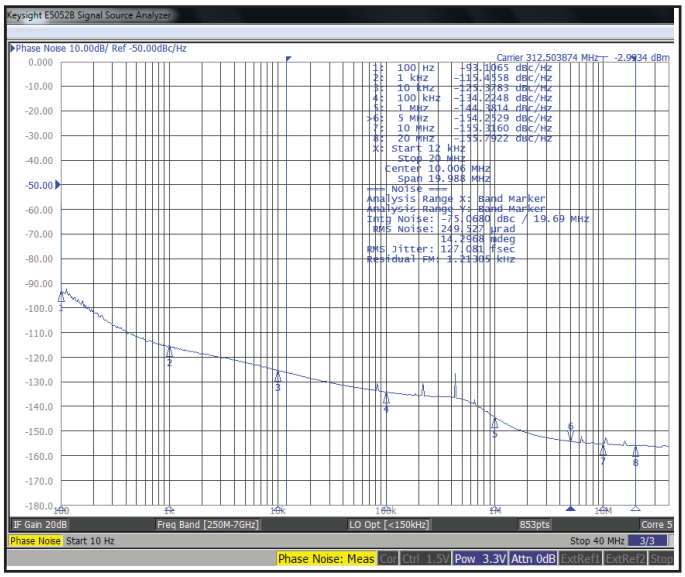
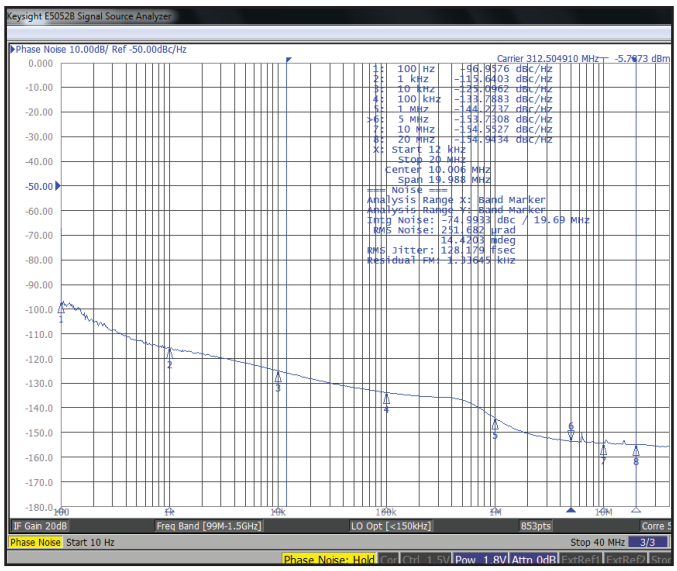
MSL = 1

Representative Phase Noise Plots

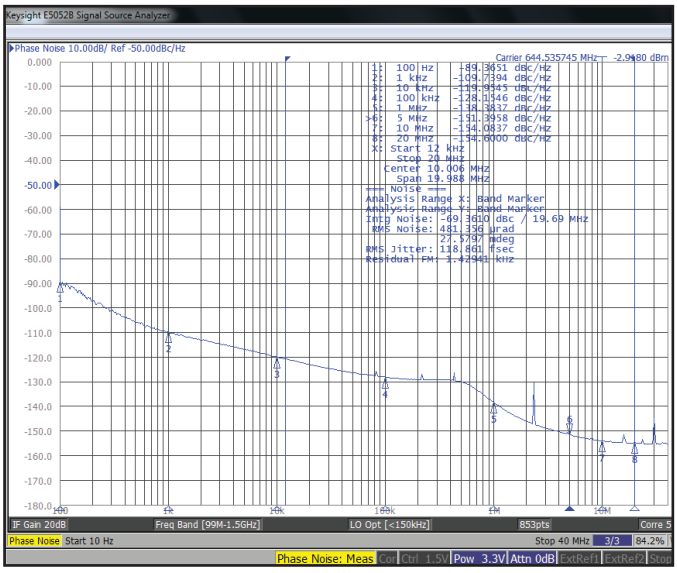
F=312.5000MHz | V_{dd}=3.3V | LVPECL
RMS Phase Jitter = 127 fsec



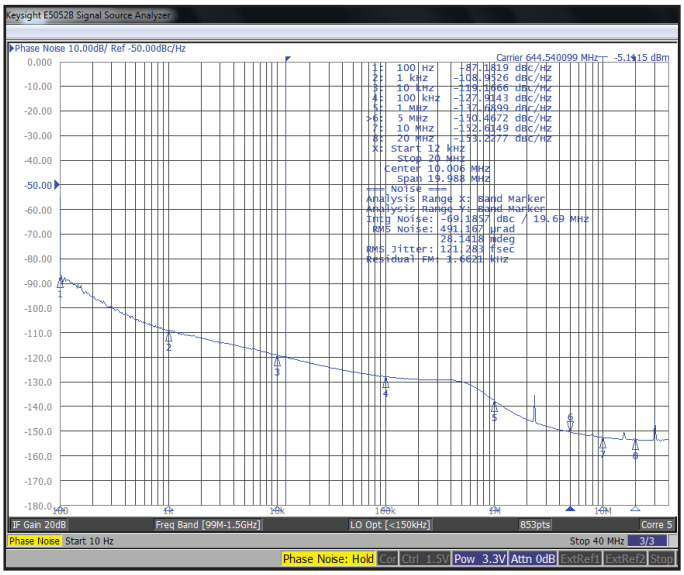
F=312.5000MHz | V_{dd}=1.8V | LVDS
RMS Phase Jitter = 128 fsec



F=644.53125MHz | V_{dd}=3.3V | LVPECL
RMS Phase Jitter = 118 fsec



F=644.53125MHz | V_{dd}=3.3V | LVDS
RMS Phase Jitter = 121 fsec



Note 9: Contact Abracon for phase noise plots at any desired combination of V_{dd}, differential output format, and carrier frequency within the available range

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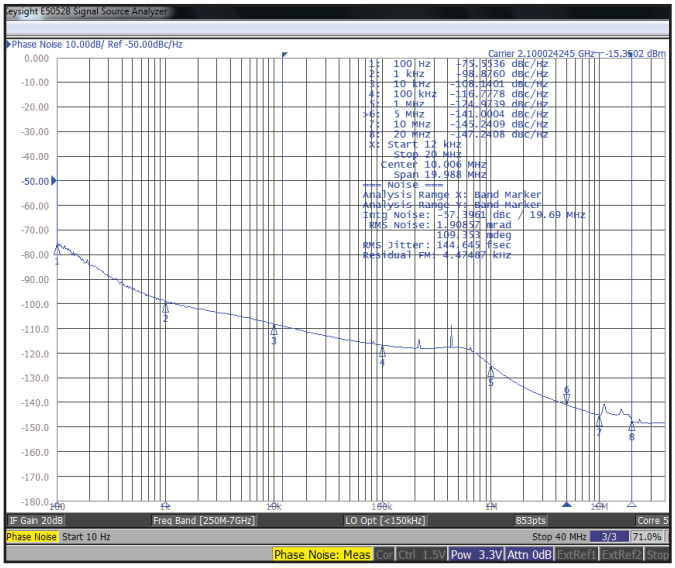
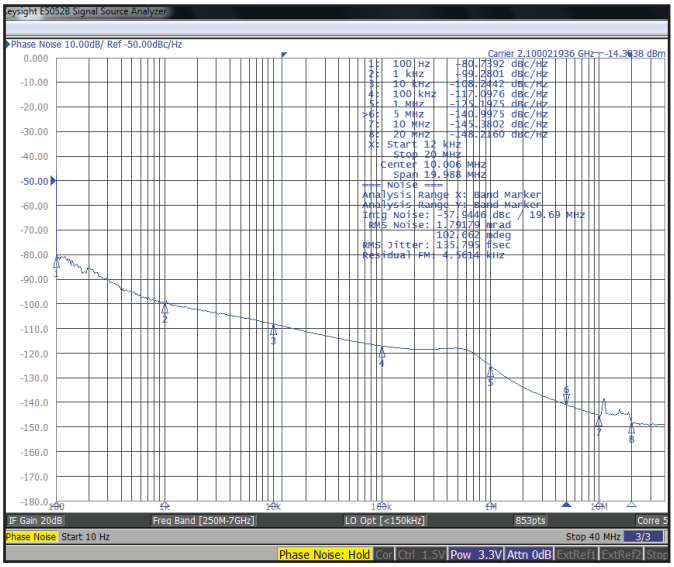
Representative Phase Noise Plots Continued

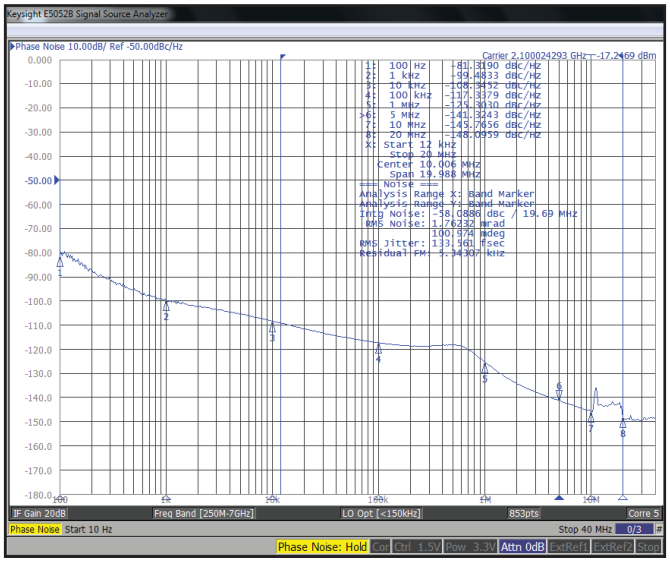
F=2100.0000MHz | V_{dd}=3.3V | LVPECL
RMS Phase Jitter = 144 fsec



F=2100.0000MHz | V_{dd}=3.3V | LVDS
RMS Phase Jitter = 135 fsec



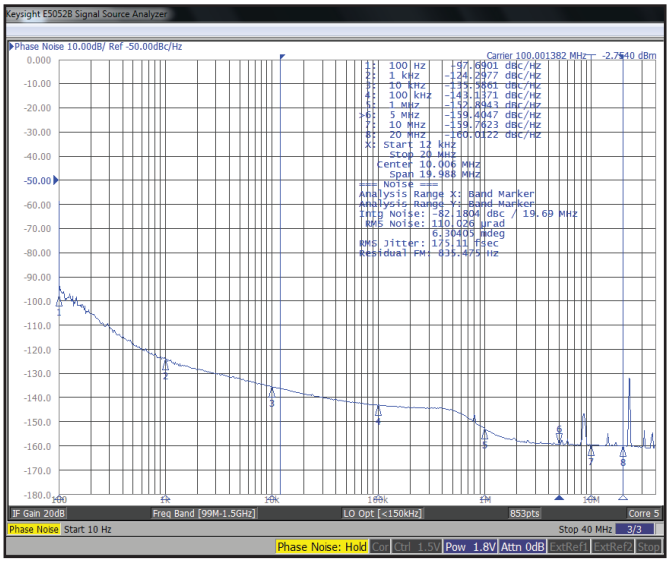
F=2100.0000MHz | V_{dd}=3.3V | CML
RMS Phase Jitter = 133 fsec



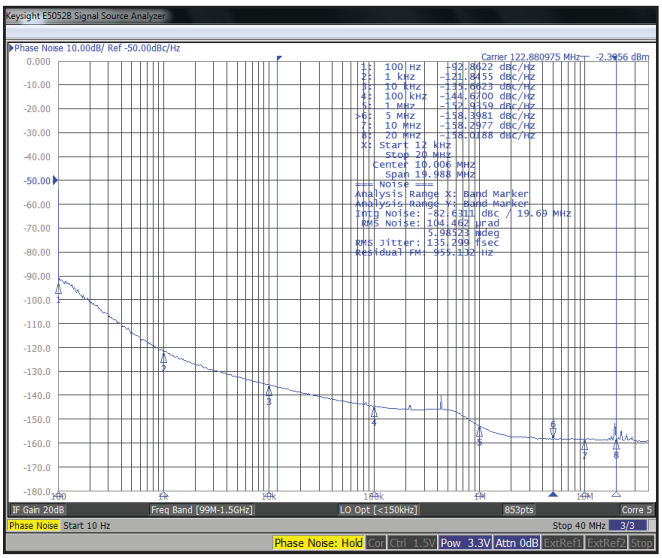
Note 9: Contact Abracon for phase noise plots at any desired combination of V_{dd}, differential output format, and carrier frequency within the available range

Representative Phase Noise Plots Continued

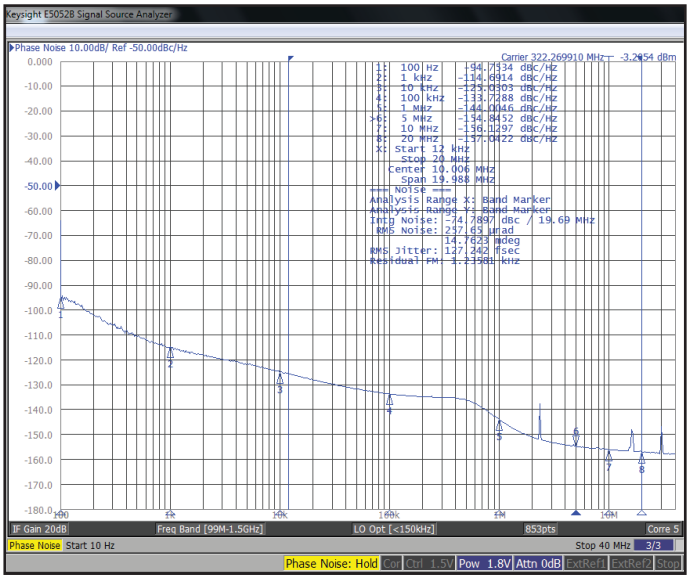
F=100.0000MHz | V_{dd}=1.8V | HCSL
RMS Phase Jitter = 175 fsec



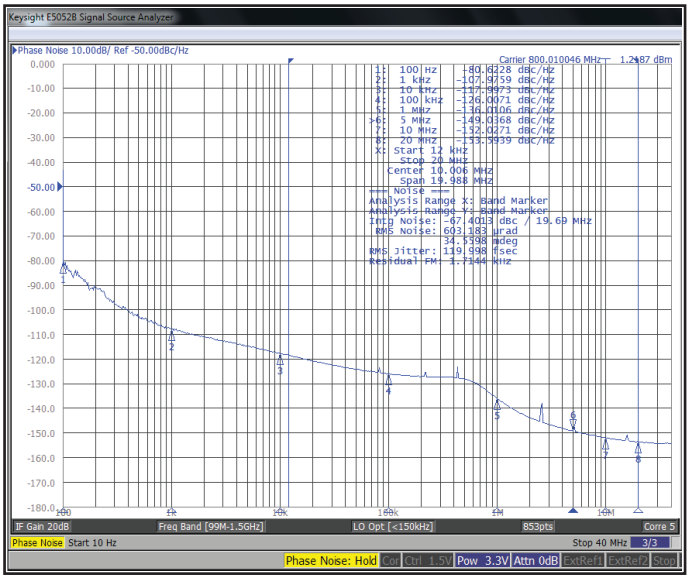
F=122.8800MHz | V_{dd}=3.3V | LVPECL
RMS Phase Jitter = 135fsec



F=322.265625MHz | V_{dd}=1.8V | HCSL
RMS Phase Jitter = 127 fsec



F=800.0000MHz | V_{dd}=3.3V | LVPECL
RMS Phase Jitter = 119 fsec



Note 9: Contact Abracon for phase noise plots at any desired combination of V_{dd}, differential output format, and carrier frequency within the available range

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RoHS/RoHS II Compliant
MSL = 1

Cross Reference to SiLabs Si545 Family

Part Number [Note 10]				
Si545	**AX5**	**Frequency (MHz)**	**Output Logic**	**Vdd (V)**
545AAA156M250BAG	AX5P**x**F1-156.2500	156.25000	LVPECL	2.5V, 3.3V
545AAA250M000BAG	AX5P**x**F1-250.0000	250.00000	LVPECL	2.5V, 3.3V
545BAA100M000BAG	AX5D**x**F1-100.0000	100.00000	LVDS	1.8V, 2.5V, 3.3V
545BAA622M080BAG	AX5D**x**F1-622.0800	622.08000	LVDS	1.8V, 2.5V, 3.3V
545AAA500M000BAG	AX5P**x**F1-500.0000	500.00000	LVPECL	2.5V, 3.3V
545AAA000127BAG	AX5P**x**F1-644.53125	644.53125	LVPECL	2.5V, 3.3V
545BAA500M000BAG	AX5D**x**F1-500.0000	500.00000	LVDS	1.8V, 2.5V, 3.3V
545AAA622M080BAG	AX5P**x**F1-622.0800	622.08000	LVPECL	2.5V, 3.3V
545BAA000127BAG	AX5D**x**F1-622.0800	622.08000	LVDS	1.8V, 2.5V, 3.3V
545AAA200M000BAG	AX5P**x**F1-200.0000	200.00000	LVPECL	2.5V, 3.3V
545BAA000274BAG	AX5D**x**F1-148.0000	148.00000	LVDS	1.8V, 2.5V, 3.3V
545AAA312M500BAG	AX5P**x**F1-312.5000	312.50000	LVPECL	2.5V, 3.3V
545AAA000274BAG	AX5P**x**F1-148.0000	148.00000	LVPECL	2.5V, 3.3V
545BAA312M500BAG	AX5D**x**F1-312.5000	312.50000	LVDS	1.8V, 2.5V, 3.3V
545AAA125M000BAG	AX5P**x**F1-125.0000	125.00000	LVPECL	2.5V, 3.3V
545AAA100M000BAG	AX5P**x**F1-100.0000	100.00000	LVPECL	2.5V, 3.3V
545BAA200M000BAG	AX5D**x**F1-200.0000	200.00000	LVDS	1.8V, 2.5V, 3.3V
545BAA125M000BAG	AX5D**x**F1-125.0000	125.00000	LVDS	1.8V, 2.5V, 3.3V
545BAA156M250BAG	AX5D**x**F1-156.2500	156.25000	LVDS	1.8V, 2.5V, 3.3V
545BAA250M000BAG	AX5D**x**F1-250.0000	250.00000	LVDS	1.8V, 2.5V, 3.3V

Note 10: The "x" in the AX5 part number is a placeholder for the supply voltage (V_{dd}) options below:
"x" = A = V_{dd}=3.3V
"x" = B = V_{dd}=2.5V
"x" = C = V_{dd}=1.8V (when applicable)

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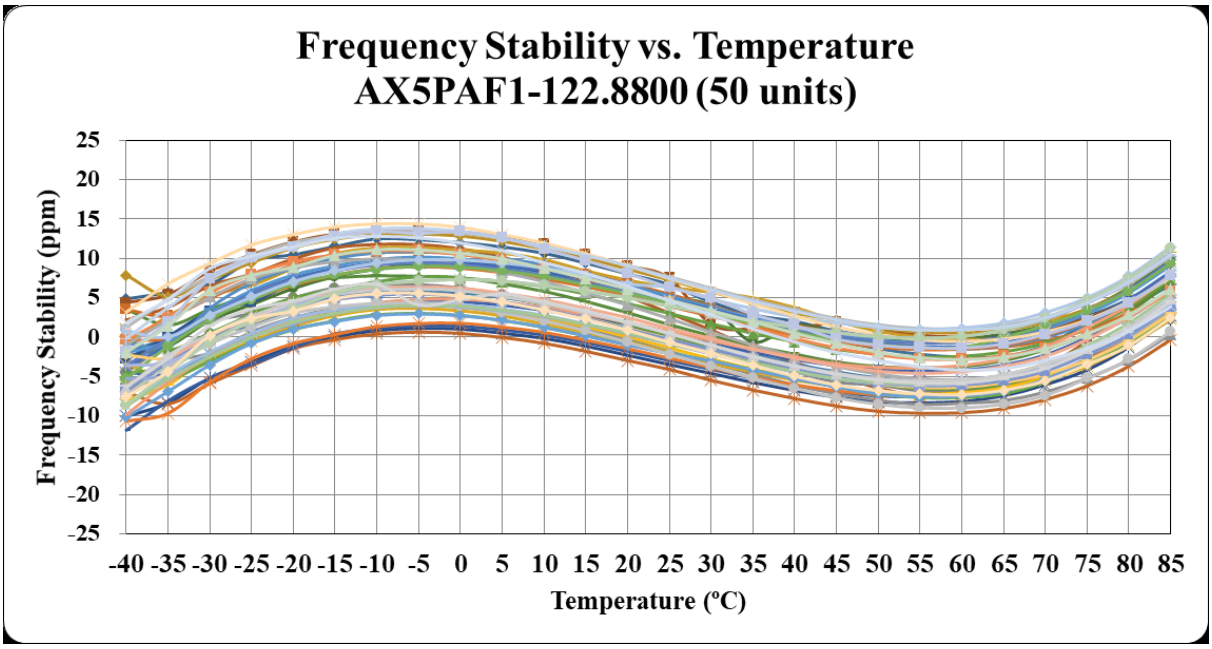
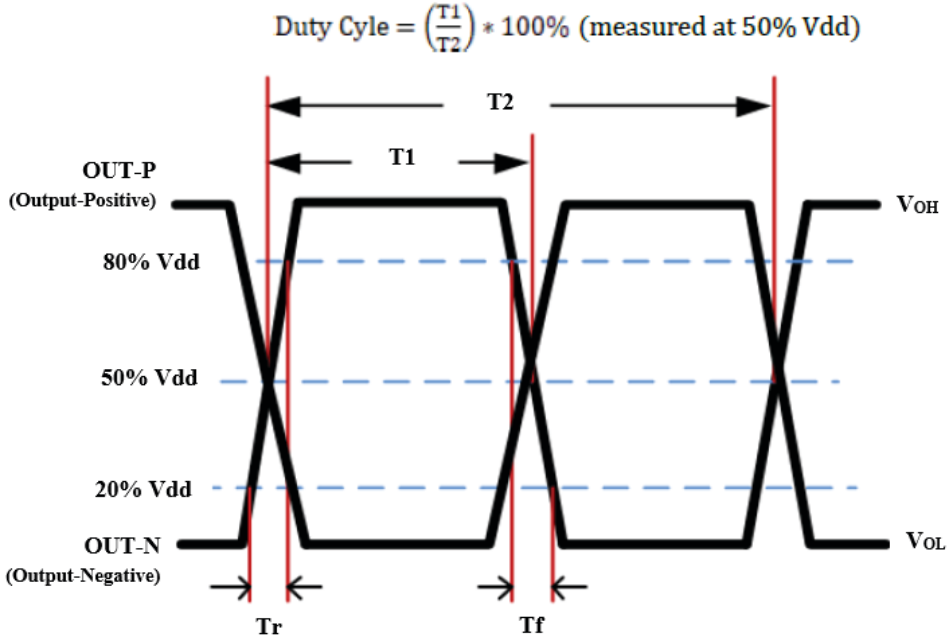
RoHS/RoHS II Compliant
MSL = 1

Typical Frequency vs. Temperature Characteristics



Differential Output Waveform



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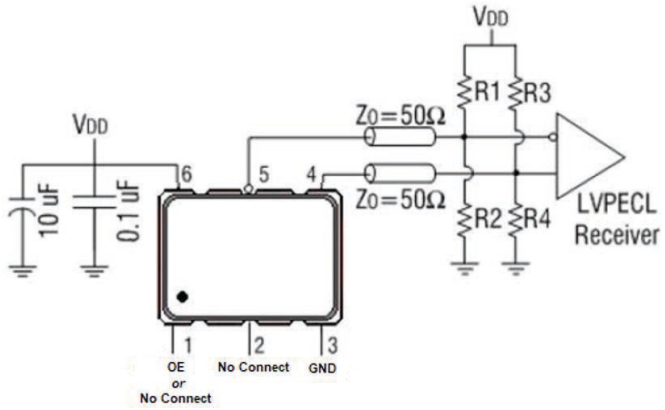
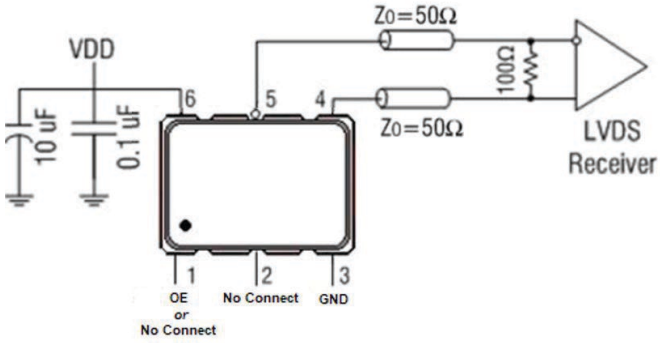
Recommended Test Circuit [Note 11]

LVPECL

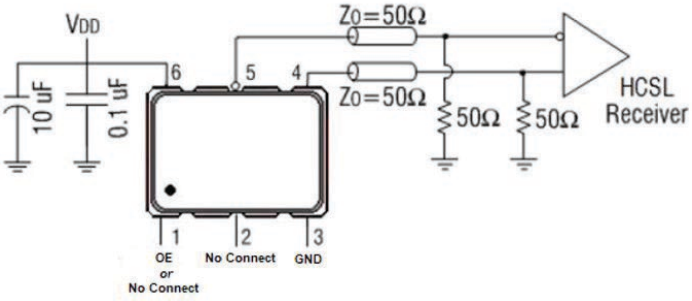


LVDS @ V_{dd} = 3.3V & 2.5V

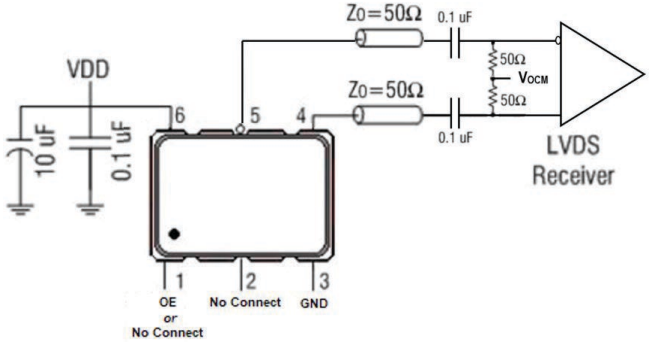


V_{dd}=3.3V: R1=R3=127Ω; R2=R4=82.5 Ω
V_{dd}=2.5V: R1=R3=250Ω; R2=R4=62.5 Ω

HCSL

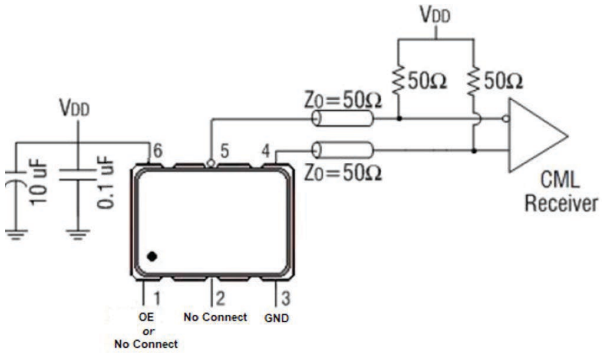


LVDS @ V_{dd} = 1.8V



The output common mode voltage, V_{OCM}, is required to be supplied externally, where V_{OCM} = 1.3V.
AC coupling needs to be implemented between the clock device (oscillator) and the receiver circuit.

CML



Note 11: Recommended test circuit images display OE Functions Option 1 & Option 2 where the OE Function is located on Pin 1
When the OE Function is located on Pin 2, then Pin 1=No Connect & Pin 2=OE or No Connect

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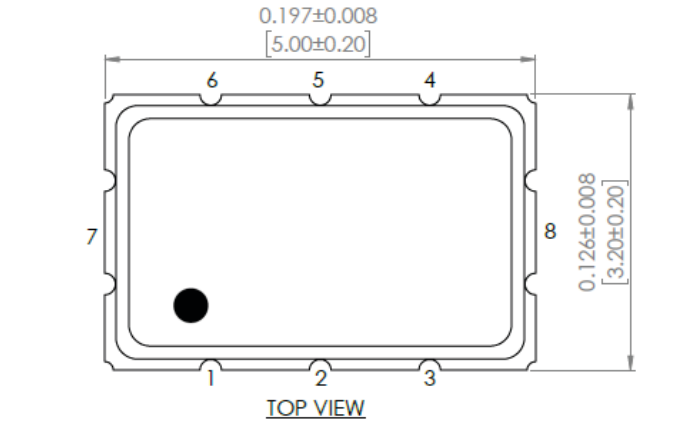
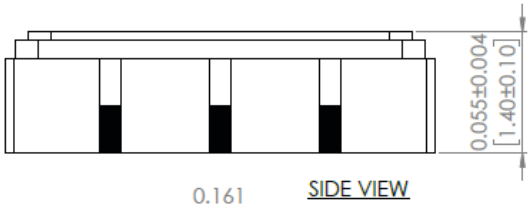
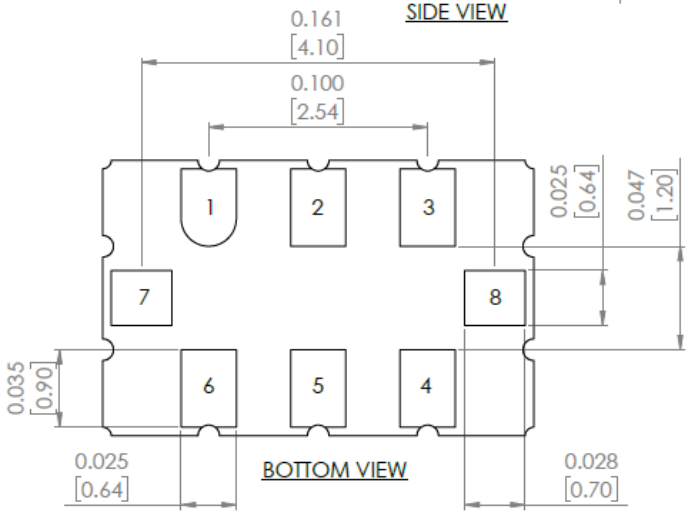
MSL = 1

Mechanical Dimensions [Note 12]

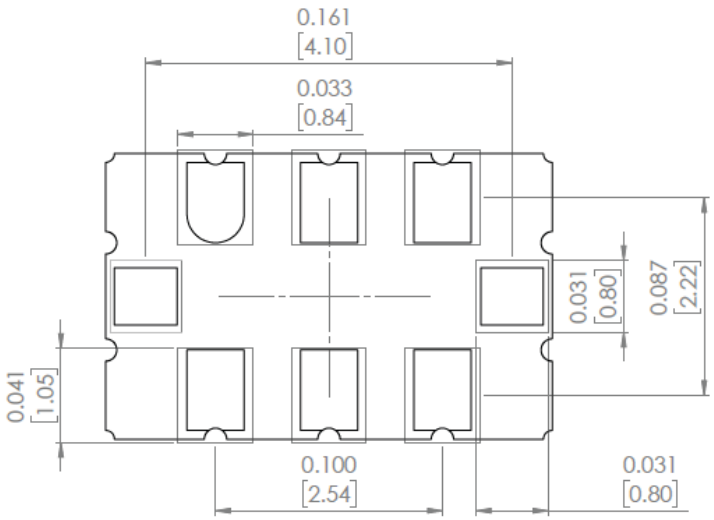






Note 12: Compatible with industry standard 5.0 x 3.2mm footprint. Pins #7 and #8 do not require a solder connection; it is not recommended to electrically connect the pins as they are for factory use only.

Recommended Land Pattern



Pin #	Function
# 1	Option 1 & 2:[Note 13] Output Enable/Disable Option 3 & 4:[Note 14] No Connect
# 2	Option 1 & 2:[Note 13] No Connect Option 3 & 4:[Note 14] Output Enable/Disable
# 3	GND
# 4	Output
# 5	Complementary output
# 6	Supply Voltage (V_{dd})
# 7	No connect
# 8	No connect

Note 13: Option 1 = Pin 1 Output Enable Active HIGH; Output Disable Active LOW
Option 2 = Pin 1 Output Enable Active LOW; Output Disable Active HIGH

Note 14: Option 3 = Pin 2 Output Enable Active HIGH; Output Disable Active LOW
Option 4 = Pin 2 Output Enable Active LOW; Output Disable Active HIGH

Dimensions: inches [mm]

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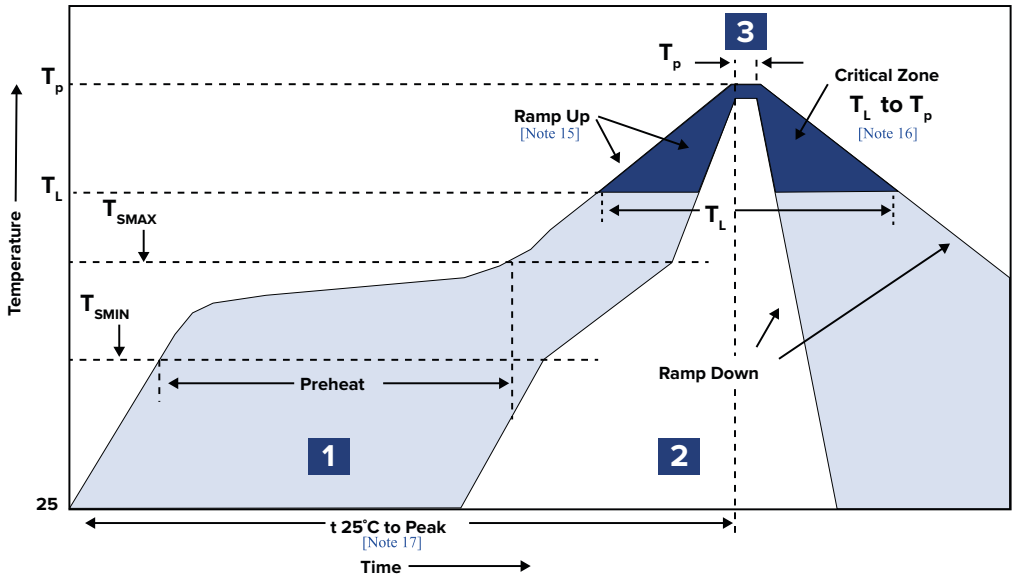
ClearClock™ | Ultra-Low Jitter & Power Optimized 5.0 x 3.2 mm XO

AX5

ESD Sensitive

5.0 x 3.2 x 1.4 mm
RoHS/RoHS II Compliant
MSL = 1

Recommended Reflow Profile [Note 18]



Zone	Description	Temperature	Time
1	Preheat / Soak	T_{SMIN} ~ T_{SMAX} 150°C ~ 200°C	60 ~ 180 sec.
2	Reflow	T_L 217°C	60 ~ 150 sec.
3	Peak heat	T_P 260°C±5°C	20 ~ 40 sec.

Note 15: Ramp Up Rate ($T_L \rightarrow T_p$) = 3°C / sec. MAX
Note 16: Ramp Down Rate ($T_p \rightarrow T_L$) = 6°C / sec. MAX
Note 17: Time 25°C to Peak Temperature (25°C $\rightarrow T_p$) = 8 minutes MAX
Note 18: Can withstand 2 times reflow
All temperatures refer to topside of the package, measured on the package body surface below.

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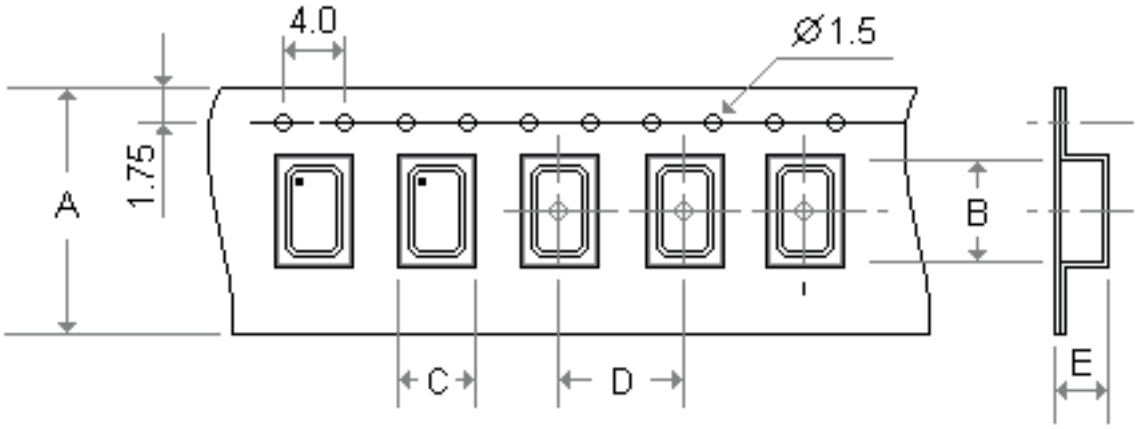
MSL = 1

Packaging

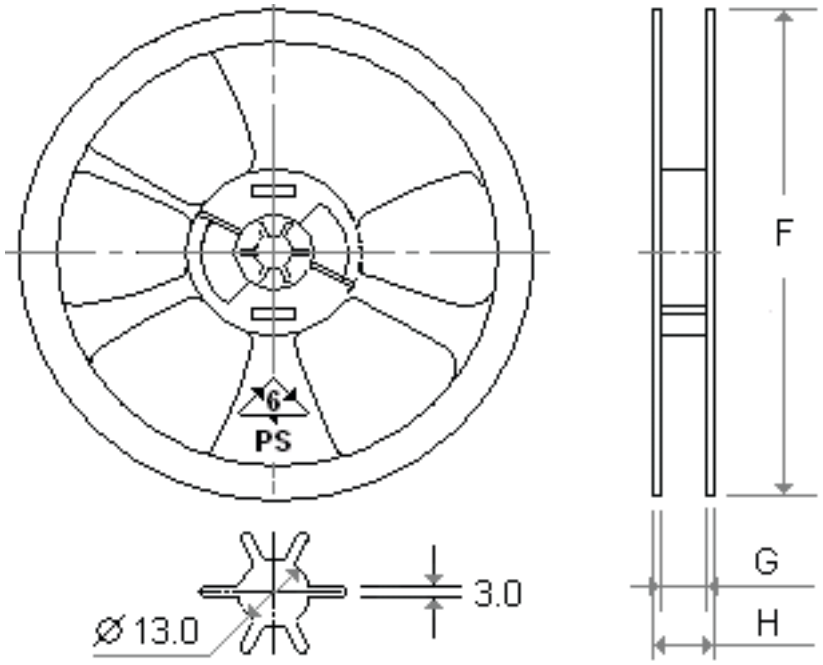
Blank = Bulk*
T = Tape & Reel 250 units/reel

(*) MOQ: 25 units

Feeding (PULL) Direction →



Tape Dimensions	
A	12.0
B	5.3
C	3.6
D	8.0
E	1.4
Reel Dimensions	
F	180.0
G	13.0
H	16.0



Dimensions: mm

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